REMARKS

Claims 29-32, 34-39, 41, 44-47, 49 and 51-64 are pending in this application. Claims 29, 36, 44, 60 and 61 have been amended. No new matter has been introduced.

Claims 29-35 stand rejected under 35 U.S.C. §112, first paragraph, as "[T]he claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art . . . to make and/or use the invention." (Office Action at 2). In particular, the Examiner asserts that the language "an electropolished patterned metal layer provided over said insulating layer . . . wherein a top of said electropolished patterned metal layer is electropolished down to said insulating layer so that said top surface of the electropolished metal layer is below or at the same level with a top surface of the insulating layer" is not described in the specification in such a way as to enable one skilled in the art to make and/or use the invention." (Office Action at 2-3). Applicant points out that claim 29 has been amended to clarify that "a top surface of said electropolished metal layer is electropolished down to said insulating layer so that said top surface of said electropolished metal layer is at the same level with a top surface of said insulating layer."

Applicant also note that the specification of the application clearly describes that the top surface of the electropolished metal layer is at the same level with the top surface of the insulating layer. The Detailed Description section emphasizes that, after the formation of the photoresist plug 66, "the resulting structure is introduced into an electropolishing system and immersed into an electrolytic chemical bath to remove the exposed platinum portions 65a, 65b formed over the second dielectric layer 25, and to form lower platinum electrode 70, as illustrated in Figure 11." (Application at 12, lines 7-11). The specification also details that "the structure of Figure 10 is electropolished for a time sufficient to allow the top surface of the lower platinum electrode 70 (Figure 11) to be recessed down to the planar surface of the second insulating layer 25."

(Application at 12, lines 11-13). Figures 11-14 also illustrate top surface of the electropolished lower platinum electrode 70 at the same level with the top surface of insulating layer 25. Thus, the subject matter of claims 29-35 is described in the specification in such a way as to enable one skilled in the art to make and/or use the invention. Applicant submits that all pending claims are now in full compliance with 35 U.S.C. § 112, first paragraph.

Claims 29-35 stand rejected under 35 U.S.C. §112, second paragraph, as "being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention." (Office Action at 3). In particular, the Examiner asserts that the language "an electropolished patterned metal layer provided over said insulating layer . . . wherein a top of said electropolished patterned metal layer is electropolished down to said insulating layer so that said top surface of the electropolished metal layer is below or at the same level with a top surface of the insulating layer" of claim 29 is "too vague because the top surface of the electropolished metal layer 70 could not be below or at the same level with a top surface of the insulating layer 24." (Office Action at 3). Applicant points out that claim 29 has been amended to clarify that the electropolished patterned metal layer is provided "within an opening of said insulating layer" and that "a top surface of said electropolished metal layer is electropolished down to said insulating layer so that said top surface of said electropolished metal layer is at the same level with a top surface of said insulating layer." Applicant submits that all pending claims are now in full compliance with 35 U.S.C. § 112, second paragraph.

Claims 29-32, 34-39, 41 and 51-64 stand rejected under 35 U.S.C. § 102 as being anticipated by Agarwal et al. (U.S. Patent No. 6,297,527) ("Agarwal"). This rejection is respectfully traversed.

The claimed invention relates to an electropolished patterned metal layer formed as part of a semiconductor device. As such, amended independent claim 29 recites a semiconductor device comprising *inter alia* "an insulating layer provided over said substrate" and "an electropolished patterned metal layer provided within an opening of said insulating layer." Amended independent claim 29 also recites that "a top surface of said electropolished metal layer is . . . at the same level with a top surface of said insulating layer."

Amended independent claim 36 recites a "memory cell" comprising *inter alia* "a transistor including a gate fabricated on a semiconductor substrate" and "an electropolished metal layer within an insulating layer provided over said substrate." Amended independent claim 36 also recites "a container capacitor including a lower electrode and a dielectric layer over said lower electrode, said lower electrode having a surface aligned over said source/drain region, said electropolished patterned metal layer forming said lower electrode, and said dielectric layer being in contact with said insulating layer."

Independent claim 55 recites a "container capacitor" comprising *inter alia* "a lower electrode provided within a first insulating layer, said lower electrode comprising an electropolished patterned metal layer having a bottom wall and vertical sidewalls extending upwardly therefrom." Independent claim 55 further recites "a second insulating layer provided over said electropolished patterned metal layer and in contact with said first insulating layer" and "an upper electrode provided over said second insulating layer."

Independent claim 59 recites a "container capacitor" comprising *inter alia* "a barrier conductive layer" and "a lower electrode . . . comprising an electropolished patterned metal layer." Independent claim 59 also recites that the electropolished

patterned metal layer has "a bottom and vertical sidewalls extending upwardly from said bottom, said lower electrode having a thickness of approximately 100 Angstroms." Independent claim 59 further recites "a dielectric material provided over said electropolished patterned metal layer and in contact with said insulating layer" and "an upper electrode provided over said dielectric material."

Amended independent claim 60 recites a "container capacitor" comprising *inter alia* "a plurality of openings provided in said insulating layer" and "a plurality of lower capacitor electrodes provided along the bottom and sidewalls of respective ones of said openings, said lower electrodes being formed as discrete electropolished metal layers." Amended independent claim 60 also recites "a dielectric layer associated with each of said discrete lower electrodes, said dielectric layer being in contact with said insulating layer."

Agarwal relates to a "high dielectric constant capacitor having a multilayer lower electrode comprising at least two layers--a platinum layer and a platinum-rhodium layer--for use in a random access memory (RAM) cell." (Abstract). According to Agarwal, "[t]he platinum layer of the lower electrode adjoins the capacitor dielectric, which is a ferroelectric or high dielectric constant dielectric such as BST, PZT, SBT or tantalum pentoxide." (Abstract). Agarwal also teaches that "[t]he platinum-rhodium layer serves as an oxidation barrier and may also act as an adhesion layer for preventing separation of the lower electrode from the substrate, thereby improving capacitor performance." (Abstract).

Agarwal does not anticipate the subject matter of claims 29-32, 34-39, 41 and 51-64. Agarwal does not disclose "a top surface of said electropolished metal layer is . . . at the same level with a top surface of said insulating layer" (claim 29) or "a second insulating layer provided over said electropolished patterned metal layer and in contact with said first insulating layer" (claim 55) or "a dielectric material provided over said

electropolished patterned metal layer and in contact with said insulating layer" (claim 59). Agarwal teaches that the top surfaces of platinum layer 74, which would arguably correspond to the "electropolished patterned metal layer" of the claimed invention, are either above or below the top surface of the insulating layer 64, which would arguably correspond to the "insulating layer" of the claimed invention, and not "at the same level with" it, as in the claimed invention. Agarwal also teaches that dielectric layer 72, which would arguably correspond to the "dielectric layer" of the claimed invention, is over and in contact with the platinum layer 74, and not "in contact with said first insulating layer," as in the claimed invention. Thus, for at least these reasons, Agarwal fails to anticipate the subject matter of claims 29-32, 34-39, 41 and 51-64, and withdrawal of the rejection of these claims is respectfully requested.

Applicant also reaffirms that the limitation "electropolished patterned metal layer" is simply not a product-by-process limitation, but rather a *resulting structure* having distinct and defined characteristics. The term "electropolished patterned" describes the physical characteristics of the metal layer in independent claims 29, 36, 44, 55, 59 and 60. Specifically, the term "electropolished patterned" is a limitation of the metal layer. Claim limitations which confer distinct and defined characteristics of a structure have been analyzed by the Federal Circuit in Hazani v. U.S. Int'l Trade Comm'n, for example. Hazani v. U.S. Int'l Trade Comm'n, 126 F.3d 1473, 44 USPQ2d 1358 (Fed. Cir. 1997). An "electropolished patterned metal layer," like the "chemically engraved" plate of Hazani, is a *resulting structure* having distinct and defined characteristics and not a product formed by a particular process. Thus, this is an additional reason why Agarwal fails to anticipate the subject matter of claims 29-32, 34-39, 41 and 51-64.

Claims 29-32, 34-39, 41, 44-47, 49 and 51-64 stand rejected under 35 U.S.C. § 102 as being anticipated by Xing et al. (U.S. Patent No. 6,090,697) ("Xing"). This rejection is respectfully traversed.

Amended independent claim 44 recites a "processor-based system" comprising *inter alia* "a container capacitor provided . . . comprising an electropolished patterned metal layer having a thickness of approximately 50 to 300 Angstroms." Amended independent claim 44 also recites that "a top surface of said electropolished patterned metal layer is at the same level with a top surface of said insulating layer."

Xing relates to a "high-selectivity via etching process" that "includes the steps of: forming an etchstop layer 840 of a material selected from the group consisting of Ti--Al, Ti--Al--N, Ta--Al, Al--N, Ti--Al/Ti--N, Ti--Al--N/Ti--N, Ta--Al/Ti--N, and Ti--Al/Ti--Al--N; forming a dielectric layer over the etchstop layer; and etching the dielectric layer with a fluorine-bearing etchant." (Abstract).

Xing fails to anticipate the subject matter of claims 29-32, 34-39, 41, 44-47, 49 and 51-64. Xing fails to disclose "a top surface of said electropolished metal layer . . . at the same level with a top surface of said insulating layer" (claim 29) or "a top surface of said electropolished patterned metal layer . . . at the same level with a top surface of said insulating layer" (claim 44). Xing is also silent about "a second insulating layer provided over said electropolished patterned metal layer and in contact with said first insulating layer" (claim 55) or about "a dielectric material provided over said electropolished patterned metal layer and in contact with said insulating layer" (claim 59). Xing also fails to disclose "an electropolished patterned metal layer" or "electropolished patterned metal layers," much less "an electropolished patterned metal layer" or "electropolished patterned metal layers" as part of capacitor structures, as in the claimed invention. As noted above, the limitation "electropolished patterned

metal layer" of independent claims 29, 36, 44, 55, 59 and 60 is not a product-by-process limitation, but rather a *resulting structure* having distinct and defined characteristics. For at least these reasons, Xing fails to anticipate the claimed invention, and withdrawal of the rejection of claims 29-32, 34-39, 41, 44-47, 49 and 51-64 is also respectfully requested.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

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